PLEASE AMEND SPECIFICATIONS:

NEW PARAGRAPHS ADDED, WITH NEW "FIGURE 5"

TO ADD UNDER "BRIEF DESCRIPTION OF THE DRAWINGS", AFTER FIG. 4 PARAGRAPH, ON PAGE 17, AND BEFORE "DESCRIPTION OF THE PREFERRED EMBODIMENTS", ON PAGE 18:

B1

Fig. 5, which is a top plan view, depicts a sketch of a cutout section of a chip or die layout, showing multiple bond pads with individual interlocking grid arrays, for each conducting bond pad formed.

TO ADD UNDER "DESCRIPTION OF THE PREFERRED EMBODIMENTS", ON PAGE 18, AFTER THE LONG FIG. 4 PARAGRAPH, ON PAGE 21-22, AND BEFORE THE FIRST PARAGRAPH ON PAGE 23:

B2 Cont'd

Referring to Fig. 5, which is a top plan view, the sketch depicts a cutout section of a chip or die layout 55, showing multiple bond pads 56, 57, 58, and 59 (arrows) with individual interlocking grid arrays 60, for each conducting bond pad formed. The interlocking grid arrays 60 are comprised of a passivating layer selected from the group consisting of silicon oxide, silicon nitride and polyimide and a conductive metal layer, selected from the group consisting of copper and aluminum. A diffusion barrier layer, underneath the conductive metal layer,

is comprised of TaN. The bond pad structures, 56, 57, 58 and 59, top views shown, are conducting bond pad formed by the interlocking grid array, and are over bond pad via contact regions (underneath the bond pads), which is approximately 100 by 100 microns square and the size of the structures are from about 10 to 25 microns in width, approximately 4 microns in height, and from about 4 to 10 in number, per conducting bond pad, thus, increasing surface area for improved adhesion. Conducting lines 51, 52, 53 and 54 are underneath the bond pads and are electrically connected to the bond pads through the bond pad via contacts, thus the bond pads are "anchored" to conducting lines, as opposed to being "un-anchored or floating".

B2 end